

A General Purpose FPGA Data Filter For Data Stream Processing

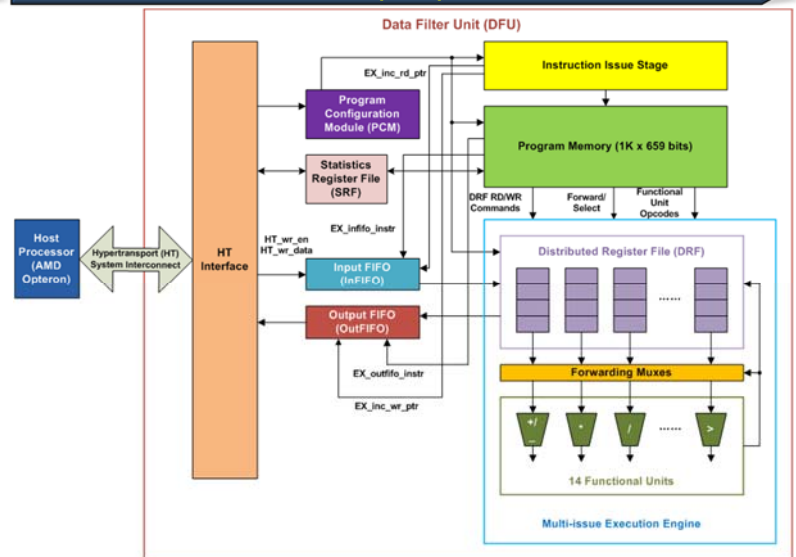
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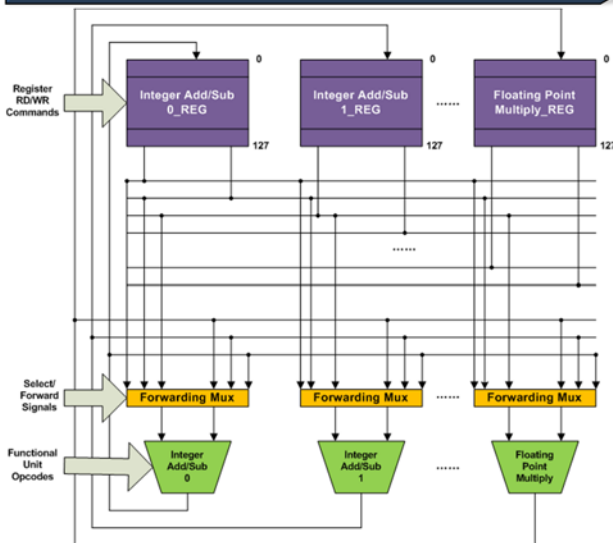
Background and Motivation

| Characteristics of Streaming Applications | Traditional Scalar Processors | DFU Approach using FPGA |
|--|---|--|
| Little memory re-use due to streaming nature | Optimized for temporal locality (using caches); Additional virtual address translation overhead | Little memory re-use advantageous to FPGA accelerators with limited Block RAMs |
| Large amounts of data parallelism possible | Loop based operators perform same operations with scalar pipelines | Data parallelism can be exploited using VLIW architectures, functional pipelining, and loop-unrolling |
| High computation to memory access ratio | Limited ILP within instruction issue window | VLIW can be tailored to meet application demands. Current architecture can perform at a peak of 7 GOPS |

Data Filter Unit (DFU) Architecture



Multi-issue Execution Engine

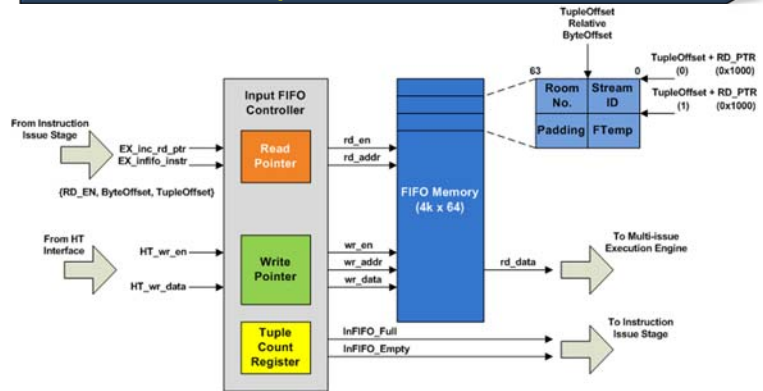


1. Novel VLIW microarchitecture to overcome the limitation of multiported memories in FPGAs called Inverted Distributed Register File (DRF)
2. Each FU can read from any register file using forwarding muxes, but write to its own dedicated 128 x 32-bit register file
3. 2 integer adder/subtractor units, 1 integer multiply unit, 2 integer to float conversion units, 1 integer comparator unit, 1 floating point adder/subtractor unit, 1 floating point multiply unit, 1 floating point divide unit, 1 floating point comparator unit, 2 floating point to integer conversion units, and 2 boolean predicate evaluation units (all units are single precision and deeply pipelined)
4. VLIW compiler written using ANTLR v3 used to convert SymQL to instruction set along with unrolled loops
5. Jump unit controls whether multi-issue execution engine executed in sequential or parallel mode

The DFU is based on a commodity DRC platform DS2004, containing two AMD Opteron 2350 quad core processors and two Opteron socket compatible DRC Reconfigurable Processor Units (RPU), all of which are connected via Hypertransport interconnects. Internal Components of the DFU:

1. HT Interface: Used to decode the HT read/write signals to internal DFU components
2. Statistics Registers: Tuples Processed Register (TPR), Stall Count Register (SCR), and Sequential Execution Count Register (SECR)
3. Input/Output FIFOs: Used to write input data streams, read output data streams
4. Program Configuration Module: Controls the program running on the multi-issue execution engine. Also used to preload program constants into the DRF
5. Instruction Issue Stage: Used to issue a wide 659-bit VLIW instruction to 14 computation units
6. Multi-issue execution engine: VLIW microarchitecture with the Distributed Register File (DRF)

Input FIFO Structure



1. Input FIFO is written by the host processor using HT write signals and is read by the DFU, which is controlled by the IIS and Program Memory
2. Output FIFO is written by the DFU and read by the host processor
3. Tuples at the head of the FIFO are selected using the current tuple pointer
4. Attributes are selected using signals (Tuple Offset, Byte Offset)
5. FIFO is implemented as a circular buffer using 4K x 64-bit block RAMs

Experimental Results

| Resources | No. of Resources | Percentile Chip Area |
|--------------------------|----------------------|----------------------|
| No. of Slice LUTs | 11806 | 5% |
| No. of Block RAMs | 49 | 17% |
| No. of DSP48Es | 2 | 1% |
| Minimum Period/Frequency | 8.189ns / 122.11 MHz | |

Synthesis Results

| | No. of Cycles | No. of Instr. Executed | Processing Time(ns) | Speedup (w.r.t. software) |
|----------------|---------------|------------------------|---------------------|---------------------------|
| Software (avg) | 3,274.03 | 1,337 | 2,430 | 1.0 |
| Hardware | 19 | 19 | 190 | 12.79 |

- 65K tuples processed
- With a single DFU running at 100MHz vs. AMD Opteron 2350 at 2GHz

Execution Costs of Software and Hardware Filters (per tuple)